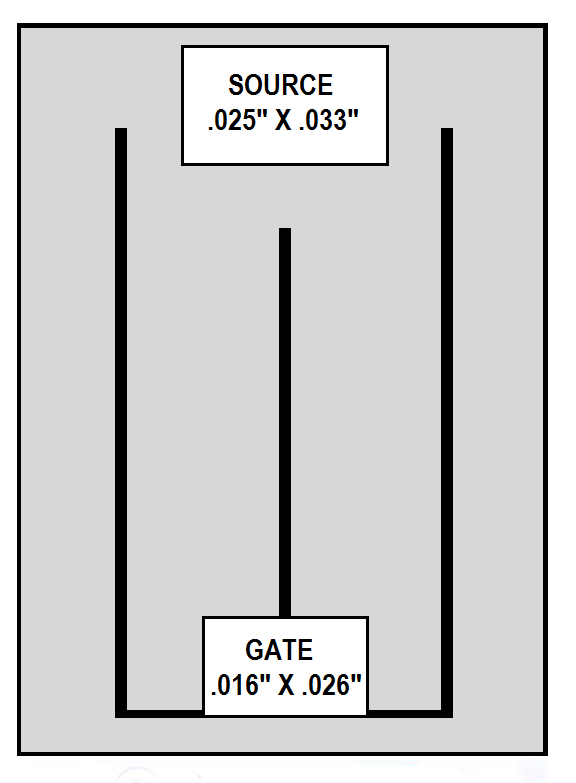
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.181”**

**.116”**



**CHIP BACK IS DRAIN**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: (See Above)**

**Backside Potential: DRAIN**

**Mask Ref: HEX 3**

**APPROVED BY: DK DIE SIZE .116” X .181” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .016” P/N: IRFC230**

**DG 10.1.2**

#### Rev B, 7/19/02